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1 An algorithm for synthesis of system-level interface circuits
Ki-Seok Chung, Rajesh K. Gupta, C. L. Liu
January 1997 **Proceedings of the 1996 IEEE/ACM international conference on Computer-aided design**
Publisher: IEEE Computer Society
Full text available: pdf(293.58 KB) Publisher Site
Additional Information: full citation, abstract, references, citings, index terms

We describe an algorithm for the synthesis and optimization of interface circuits for embedded system components such as microprocessors, memory ASIC, and network subsystems with fixed interfaces. The algorithm accepts the timing characteristics of two system components as input, and generates a combinational interface (glue logic) circuit. The algorithm consists of two parts. In the first part, we determine the direct pin-to-pin connections in the interface circuit employing a 0/1 ILP formulati ...

Keywords: Interface Synthesis, System-Level Design Issues, Algorithm, Optimization

2 Testing and Debugging Custom Integrated Circuits
Edward H. Frank, Robert F. Sproull
December 1981 **ACM Computing Surveys (CSUR)**, Volume 13 Issue 4
Publisher: ACM Press
Full text available: pdf(2.25 MB)
Additional Information: full citation, references, citings, index terms

3 International standards for data communications: A status report
Ira W. Cotton, Harold C. Folts
September 1977 **Proceedings of the fifth symposium on Data communications**
Publisher: ACM Press
Full text available: pdf(1.13 MB)
Additional Information: full citation, abstract, references, index terms

Recent developments in data communications standards have been patterned on a hierarchical approach to communications system architecture. A number of independent levels have been identified, and standards development has proceeded at its own pace within each level. These levels are identified and recent progress at standardization is discussed for each.

4 FORM: A Frame-Oriented Representation Method for Digital Telecommunication System Design

K. Shirakawa, K. Higuchi, T. Miyazaki, K. Hayashi, K. Yamada

March 1996 **Proceedings of the 1996 European conference on Design and Test**

Publisher: IEEE Computer Society

Full text available: pdf(683.44 KB) Publisher Site Additional Information: full citation, abstract, citings

This paper proposes a new design method called FORM (Frame-Oriented Representation Method) for digital telecommunication systems with the aiming of efficient system design and development. FORM has the unique feature wherein timing design and function design are performed independently. FORM can translate system-level specifications at the behavioral level into RTL. This method is applied to the SDH/ATM interface and it is proved that FORM relaxes design complications and simplifies system desig ...

Keywords: Telecommunication, Specification, System design, ATM, High-level design, multimedia, Frame

5 Schematic-based lumped parameterized behavioral modeling for suspended MEMS

Qi Jing, Tamal Mukherjee, Gary K. Fedder

November 2002 **Proceedings of the 2002 IEEE/ACM international conference on Computer-aided design ICCAD '02**

Publisher: ACM Press

Full text available: pdf(243.93 KB) Additional Information: full citation, abstract, references, index terms

Schematic-based lumped parameterized behavioral modeling and simulation methodologies have become available since the emergence of analog HDLs. They greatly ease iterative hierarchical multi-domain simulation, which is critical to the design of MEMS. NODAS is one of such tools, with models written in VerilogA and simulation performed within the Cadence framework.This paper focuses on several key modeling issues in NODAS, including schematic representation, element communication, linear, nonlinea ...

Keywords: MEMS, behavioral, electrostatic gap, lumped, nonlinear beam, parameterized, schematic-based

6 Unconventional interconnects: Optical solutions for system-level interconnect

Ian O'Connor

February 2004 **Proceedings of the 2004 international workshop on System level interconnect prediction**

Publisher: ACM Press

Full text available: pdf(873.11 KB) Additional Information: full citation, abstract, references, index terms

Throughput, power consumption, signal integrity, pin count and routing complexity are all increasingly important interconnect issues that the system designer must deal with. Recent advances in integrated optical devices may deliver alternative interconnect solutions enabling drastically enhanced performance. This paper begins by outlining some of the more pressing issues in interconnect design, and goes on to describe system-level optical interconnect for inter- and intra-chip applications. Inte ...

Keywords: interconnect technology, optical interconnect, optical network on chip

7 Design aids and hardware testing of microprocessor system circuit packs

J. Grason
February 1977 **Proceedings of the Symposium on Design Automation and Microprocessors**
Publisher: IEEE Press
Full text available: pdf(444.58 KB) Additional Information: full citation, abstract, references, index terms

In this paper the hardware testing of microprocessor system circuit packs is treated, with particular emphasis on the role of automatic design aids in this process. Specific problems of implementing these tests on automatic test machines are also considered. Goals and methods of testing in this context are discussed, with special attention paid to functional simulation as a design aid. Several unique problems this type of testing are discussed, including tri-state busses, dynamic RAMs, PROM ...

8 Integrated computer aided design, documentation and manufacturing system for PCB electronics
Mikko Tervonen, Hannu Lehikoinen, Timo Mukari
June 1983 **Proceedings of the 20th conference on Design automation**
Publisher: IEEE Press
Full text available: pdf(648.79 KB) Additional Information: full citation, abstract, references, index terms

This paper describes an integrated computer aided design, documentation and manufacturing system, which assures data integrity from physical design to manufacturing with the aid of one phase data input and integrated parts data base. Unique features of the system are comprehensive documentation support for PCB electronics, one-phase user friendly data input, intensive input data checking, support for part and document numbering and PCB numbering, user definable document formats and language ...

9 CGALA-a multi technology Gate Array Layout system
L. F. Todd, J. M. Hansen, S. V. Pantulu, J. L. Barron, D. J. Gilbert, R. J. Anderson, A. K. Biyani
January 1982 **Proceedings of the 19th conference on Design automation**
Publisher: IEEE Press
Full text available: pdf(1.18 MB) Additional Information: full citation, abstract, references, citings, index terms

This paper describes the Computerized Gate Array Layout system (CGAL), a general purpose tool developed at Sperry Univac to provide efficient and reliable automated layouts for a variety of master slice arrays. The system contains algorithms for the construction of initial placement, placement improvement, global routing, channel routing and planar routing. The system also provides for user interaction through a design language and graphical output. A wide range of device types e ...

10 Circuit effects in static timing: VeriCDF: a new verification methodology for charged device failures
Jaesik Lee, Ki-Wook Kim, Sung-Mo Kang
June 2002 **Proceedings of the 39th conference on Design automation**
Publisher: ACM Press
Full text available: pdf(1.01 MB) Additional Information: full citation, abstract, references, index terms

A novel tool for full-chip verification is reported for CDM-ESD protection. Until recently, ESD protection has been simulated in device level, leading to the well known limitations on capturing global features such as the power protection circuits and package parasitics. In practice, fatal failures occur due to unexpected discharged paths in multi-power supply chips, which can only be verified by chip-level simulation. Associated with the new concept of macromodelling, hierarchical approach prov ...

Keywords: modeling, reliability, simulation

11 PixelFlow: the realization

John Eyles, Steven Molnar, John Poulton, Trey Greer, Anselmo Lastra, Nick England, Lee Westover

August 1997 **Proceedings of the ACM SIGGRAPH/EUROGRAPHICS workshop on Graphics hardware**

Publisher: ACM Press

Full text available: pdf(1.54 MB) Additional Information: full citation, references, citings, index terms

Keywords: compositing, deferred shading, object-parallel, rendering, scalable

12 TTL circuits for a 4-valued bus a way to reduce package and interconnections

Daniel Etiemble

January 1978 **Proceedings of the eighth international symposium on Multiple-valued logic**

Full text available: pdf(462.97 KB) Additional Information: full citation, abstract, references, index terms

This paper presents voltage mode multi-valued circuits to define a 4-valued bus. Two different versions are presented: TTL circuits for a 4-valued open collector bus, and TTL circuits for a 4-valued + high impedance bus. Some dynamic characteristics are shown. With usual load of a bus, the supplementary delay is less than 55 ns.

13 Using Java to design and test hardware circuits over a classroom network

Michael J Jipping, Steve Marlowe, Alexander Sherstov

February 2002 **ACM SIGCSE Bulletin , Proceedings of the 33rd SIGCSE technical symposium on Computer science education SIGCSE '02**, Volume 34 Issue 1

Publisher: ACM Press

Full text available: pdf(418.08 KB) Additional Information: full citation, abstract, references, citings

A crucial part of the Computer Organization course is the design and analysis of hardware circuits. To teach this part of the course efficiently and to involve the entire class in the design of circuits, we have designed the SCAN system. Starting with a textual specification of a circuit, SCAN generates Java classes that can be used to simulate the way the circuit works. These circuits can be simulated locally or can join with other circuits to simulate larger machine function over a network. Th ...

14 Session 4A: Simulation: Collecting data for Markov models of error patterns on data communications links

Wayne D. Smith

April 1992 **Proceedings of the 30th annual Southeast regional conference**

Publisher: ACM Press

Full text available: pdf(289.96 KB) Additional Information: full citation, abstract, references

Rome Laboratory is currently in the process of procuring Error Injector Units (EIU) to model the error behavior of data communications channels. A major component of this effort deals with finding Markov models that will simulate the behavior of these channels. This paper reports on the results of a Summer Faculty Research Fellowship to find Markov tables to load into the EIUs. A portion of the research involved searching current literature for Markov tables or error gap data. Alternative approa ...

15 A data architecture for an uncertain design and manufacturing environment

Thomas R. Smith
June 1985 **Proceedings of the 22nd ACM/IEEE conference on Design automation**
Publisher: ACM Press

Full text available: pdf(724.52 KB) Additional Information: full citation, abstract, references, citings, index terms

Traditional methods for resistance calculation suffer from some unfavourable features, that make them uncomfortable to use. Although requiring a lot of manual processing, they are rather inaccurate and often claim for severe artwork restrictions (e.g. orthogonal geometry)which conflict with the desire for most dense layouts. This paper describes a resistance calculation program called REX (Resistance Extractor), which is based on the well-known Finite Element Method (FEM) ...

16 CDMA/FDMA-interconnects for future ULSI communications

M. F. Chang
May 2005 **Proceedings of the 2005 IEEE/ACM International conference on Computer-aided design ICCAD '05**
Publisher: IEEE Computer Society
Full text available: pdf(406.91 KB) Additional Information: full citation, abstract

Future inter- and intra-ULSI interconnect systems demand extremely high data rates as well as bidirectional multi-I/O concurrent service, reconfigurable computing/processing architecture, and total compatibility with mainstream silicon SOC (system-on-chip) and SIP (system-in-package) technologies. In this talk, we review recent advances in CDMA and FDMA interconnect schemes that promise to meet all of the above system requirements. The physical transmission line is no longer limited to a direct- ...

17 Energy-aware system design: A survey of techniques for energy efficient on-chip communication

Vijay Raghunathan, Mani B. Srivastava, Rajesh K. Gupta
June 2003 **Proceedings of the 40th conference on Design automation**
Publisher: ACM Press

Full text available: pdf(94.50 KB) Additional Information: full citation, abstract, references, citings, index terms

Interconnects have been shown to be a dominant source of energy consumption in modern day System-on-Chip (SoC) designs. With a large (and growing) number of electronic systems being designed with battery considerations in mind, minimizing the energy consumed in on-chip interconnects becomes crucial. Further, the use of nanometer technologies is making it increasingly important to consider reliability issues during the design of SoC communication architectures. Continued supply voltage scaling ha ...

Keywords: communication architectures, energy efficient design, low power design, power management, system-on-chip design

18 Nano and Emerging Technologies: Multi-GHz SiGe design methodologies for reconfigurable computing

Kuan Zhou, John F. McDonald
April 2005 **Proceedings of the 15th ACM Great Lakes symposium on VLSI**
Publisher: ACM Press
Full text available: pdf(304.70 KB) Additional Information: full citation, abstract, references, index terms

A high-speed and low-power Field Programmable Gate Array (FPGA) is the dream of digital designers. The availability of Silicon Germanium (SiGe) Heterojunction Bipolar Transistor (HBT) devices has opened a door for GHz FPGAs [3, 4]. In the past, high static

power consumption discouraged the significant scale-up of bipolar FPGAs. This paper details new ideas to reduce power and layout area in designing high-speed SiGe BiCMOS FPGAs. The paper explains new methods to reduce circuitry and utilize nov ...

Keywords: CLB, FPGA, SiGe, virtex

19 REYSM, a high performance, low power multi-processor bus

J. D. Nicoud, K. Skala

June 1986 **ACM SIGARCH Computer Archi tecture News , Proceedings of the 13th annual international symposium on Computer architecture ISCA '86**, Volume 14 Issue 2

Publisher: IEEE Computer Society Press, ACM Press

Full text available: pdf(431.61 KB) Additional Information: full citation, abstract, references, citings, index terms

In order to build lower cost multimicroprocessor systems, a narrow synchronous bus (15 active lines) is proposed. It multiplexes address and data on 8 bits, and arbitrates in two pipe-lined cycles on four lines. Due to the 20 to 40 MHz bus clock, and the pipelined control logic, the performances are equivalent to Multibus-2, IEEE-P896 and similar 32-bit buses.For the implementation, cards are disposed radially around a special connector. The very short co ...

20 Advances in accelerated simulation: A fast hardware/software co-verification method for system-on-a-chip by using a C/C++ simulator and FPGA emulator with shared register communication

Yuichi Nakamura, Kouhei Hosokawa, Ichiro Kuroda, Ko Yoshikawa, Takeshi Yoshimura

June 2004 **Proceedings of the 41st annual conference on Design automation**

Publisher: ACM Press

Full text available: pdf(1.03 MB) Additional Information: full citation, abstract, references, index terms

This paper describes a new hardware/software co-verification method for System-On-a-Chip, based on the integration of a C/C++ simulator and an inexpensive FPGA emulator. Communication between the simulator and emulator occurs via a flexible interface based on shared communication registers. This method enables easy debugging, rich portability, and high verification speed, at a low cost. We describe the application of this environment to the verification of three different complex commercial SoCs ...

Keywords: C/C++ simulator, FPGA emulation, co-verification

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